We claim:

1. A circuit comprising an input terminal for connection to a voltage source having first and second levels and a transition between the levels, a driver including first and second opposite conductivity type transistors, each including a control electrode and a path switched on and off in response to the control electrode voltage being on opposite sides of a threshold, the first and second transistor paths being connected in series across opposite power supply terminals, and pulse shaping circuitry for (a) causing the first and second transistor paths to be respectively (i) on and off while the voltage source has the first level and (ii) off and on while the voltage source has the second level, and (b) preventing both paths from being on simultaneously, the circuitry including a first resistive impedance and first shunt capacitor, the first impedance being connected for supplying current to the first capacitor and the first transistor control electrode, the first capacitor being connected across the first transistor control electrode and a first of the power supply terminals.

2. The circuit of claim 1 wherein said first and second transistors are respectively a PFET and an NFET and said at least one capacitor comprises a field effect device.

3. The circuit of claim 2 wherein said resistive impedance, PFET, NFET and said at least one capacitor are included on an integrated circuit chip, and said resistive impedance comprises a resistor.

4. The circuit of claim 1 wherein the circuitry further includes a second resistive impedance and a second shunt capacitor, the second resistive

impedance being connected for supplying current to the second shunt capacitor and the control electrode of the second transistor, the second shunt capacitor being connected across the control electrode of the second transistor and a second of the power supply terminals.

5. The circuit of claim 4 wherein the first and second transistors are respectively a PFET and an NFET and the first and second shunt capacitors are respectively an NFET and a PFET.

6. The circuit of claim 5 wherein the first and second transistors, the first and second resistive impedances, and the first and second shunt capacitors are included on an integrated circuit chip, the first and second resistive impedances including first and second resistors.

7. The circuit of claim 5 further including first and second switching circuits each having (a) an input terminal for enabling the first and second switching circuits to be simultaneously responsive to the voltage at the input terminal and (b) an output terminal, the output terminal of the first switching circuit being connected so current can flow via a first DC path between (a) the first power supply terminal and (b) the first shunt capacitor and the control electrode of the first transistor, the output terminal of the second switching circuit being connected so current can flow via a second DC path between (a) the second power supply terminal and (b) the second shunt capacitor and the control electrode of the second transistor, the first and second paths respectively including the first and second resistive impedances.

8. The circuit of claim 7 wherein the first and second transistors are field effect transistors, the first and second switching circuits respectively include first and second inverters having field effect transistors, and the first and second capacitors comprise field effect devices.

9. The circuit of claim 8 wherein all of the field effect transistors and devices are included on an integrated circuit chip including first and second resistors respectively comprising the first and second resistive impedances connected in circuit with the first and second field effect transistors and the first and second inverters.

10. The circuit of claim 9 wherein the first and second resistors are respectively included in the first and second inverters.

11. The circuit of claim 10 wherein the first and second transistors are respectively a PFET and an NFET, each of the inverters including a PFET and an NFET, the PFET and NFET of each inverter having a source drain path and a gate electrode having a connection to the input terminal so that the gate electrodes of the PFETs and NFETs of the inverters are driven in parallel by the voltage at the input terminal, the output terminal of each of the inverters being between the source drain paths of the PFET and NFET thereof.

12. The circuit of claim 11 wherein the first resistor is connected between the source drain path of the NFET of the first inverter and the output terminal of the first inverter, the second resistor being connected between the source drain path of the PFET of the second inverter and the output terminal of the second inverter.

13. The circuit of claim 12 wherein the first and second capacitors respectively include an NFET and a PFET.

14. A circuit comprising an input terminal for connection to a voltage source having first and second levels and a transition between the levels, a driver including first and second opposite conductivity type transistors, each including a control electrode and a path switched on and off in response to a voltage applied to the control electrode being on opposite sides of a threshold, the first and second transistor paths being connected in series across opposite power supply terminals, an output terminal between the paths, pulse shaping circuitry connected between the input terminal and the control electrodes for (a) causing the paths of the first and second transistors to be respectively (i) on and off while the voltage source has the first level and (ii) off and on while the voltage source has the second level, and (b) preventing the paths of the first and second transistors from being on simultaneously, the circuitry including: (a) first and second switching circuits to be connected to be simultaneously responsive to the voltage at the input terminal, the first and second switching circuits respectively including output terminals having DC connections to the control electrodes of the first and second transistors; and (b) first and second capacitors respectively having DC connections between (i) the first control electrode and the first power supply terminal and (ii) the second control electrode and the second power supply terminal, the first switching circuit including a first resistive impedance for supplying current from the first power supply terminal to the control electrode of the first transistor and the first capacitor while the voltage at the input terminal

has the first level, the first switching circuit being arranged for supplying a voltage substantially equal to the voltage at the second power supply terminal to (i) the control electrode of the first transistor and (ii) the first capacitor while the voltage at the first terminal has the second level; the second switching circuit including a second resistive impedance for supplying current from the second power supply terminal to the control electrode of the second transistor and the second capacitor while the voltage at the input terminal has the second level, the second switching circuit being arranged for supplying a voltage substantially equal to the voltage at the first power supply terminal to (i) the control electrode of the second transistor and (ii) the second capacitor while the voltage at the first terminal has the first level.

15. The circuit of claim 14 wherein the first switching circuit comprises a first inverter including third and four transistors respectively switched on and off in response to the voltage at the input terminal respectively having first and second values, the first inverter including the first resistive impedance for supplying current from the first power supply terminal to the control electrode of the first transistor and the first capacitor while the third transistor is switched on; the second switching circuit comprises a second inverter including fifth and sixth transistors respectively switched on and off in response to the voltage at the input terminal respectively having first and second values, the second inverter including a second resistive impedance for supplying current from the second power supply terminal to the control electrode of the second transistor and the second capacitor while the sixth transistor is switched on.

16. The circuit of claim 15 wherein the fourth and fifth transistors while switched on are connected to supply voltages substantially at the second and first power supply terminals to the control electrodes of the first and second transistors and the first and second capacitors, respectively.

17. The circuit of claim 16 wherein all the transistors and capacitors are field effect devices.

18. The circuit of claim 17 wherein all the transistors and capacitors are included on an integrated circuit chip, the first and second resistive impedances including first and second resistors on the chip.

19. A method of operating a driver including first and second opposite conductivity type transistors, each including a control electrode and a path controlled in response to a voltage applied to the control electrode, the paths of the first and second transistors being connected in series across opposite power supply terminals, an output terminal between the series connected paths, first and second capacitors respectively connected in shunt with the control electrodes, the method comprising: during a first interval: turning on and off the paths of the first and second transistors, respectively, while the second capacitor is charged and the first capacitor is discharged by applying (a) a first voltage having a first value to the control electrode of the first transistor, (b) the first voltage value across the second capacitor, and (c) a second voltage having the first value to the control electrode of the second transistor; during a second interval: turning off and on the paths of the first and second transistors, respectively, while the second capacitor is discharged and the first capacitor is

charged by applying (a) the second value of the first voltage to the control electrode of the first transistor, (b) the first voltage value across the first capacitor, and (c) the second value of the second voltage to the control electrode of the second transistor; during an initial portion of a first transitional period between the first and second intervals: turning off the path of the first transistor while maintaining the path of the second transistor off by changing the first voltage from the first value toward the second value while the first capacitor remains substantially discharged and the second capacitor remains substantially charged; during a second portion of the first transitional period turning on the path of the second transistor while maintaining the path of the first transistor off by changing the charge on the second capacitor so that there is a change in the value of the second voltage from the first value toward the second value; during an initial portion of a second transitional period between the second and first intervals: turning off the path of the second transistor while maintaining the path of the first transistor off by changing the second voltage from the second value toward the first value while the second capacitor remains substantially discharged and the first capacitor remains substantially charged; and during a second portion of the second transitional period turning on the path of the first transistor while maintaining the path of the second transistor off by changing the charge on the first capacitor so that there is a change in the value of the first voltage from the second value toward the first value.